EXHIBIT 7

[redacted]

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2022-00999
Patent 11,232,054 B2

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory module comprising:
1.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
1.c	a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;
1.d	[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and [3] a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections, [4] wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and [5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.
2.a	2. The memory module of claim 1, wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude; and
2.b	wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes.
3	3. The memory module of claim 1, wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts.
4.a	4. The memory module of claim 1, further comprising:

Ref. #	Listing of Challenged Claims
4.b	a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage,
4.c	wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.
5.a	5. The memory module of claim 4, further comprising:
5.b	a controller coupled to the voltage monitor circuit;
5.c	wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
6.a	6. The memory module of claim 1, further comprising:
6.b	a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage,
6.c	wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.
7.a	7. The memory module of claim 6, further comprising:
7.b	a controller coupled to the voltage monitor circuit;
7.c	wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
8.a	8. The memory module of claim 1, further comprising:
8.b	a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections,
8.c	wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller.

Ref. #	Listing of Challenged Claims
9.a	9. The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage, and
9.b	wherein the first predetermined threshold voltage is above a specified operating voltage.
10	10. The memory module of claim 9, wherein the first predetermined threshold voltage is ten percent above the specified operating voltage.
11.a	11. The memory module of claim 9, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage, and
11.b	wherein the second predetermined threshold voltage is below the specified operating voltage, and
11.c	wherein the memory module transitions from a first operable state to a second operable state in response to the signal.
12	12. The memory module of claim 11, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage.
13	13. The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage.
14	14. The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system.
15	15. The memory module of claim 1, wherein two of the at least three buck converters are configured to operate as a dual-buck converter.
16.a	16. A memory module comprising:
16.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;
16.c	a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

Ref. #	Listing of Challenged Claims
16.d	[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, [3] the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages; and
16.e	[1] a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage, [2] wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.
17	17. The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage.
18.a	18. The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and
18.b	wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.
19.a	19. The memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit, and
19.b	wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.
20.a	20. The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and

Ref. #	Listing of Challenged Claims
20.b	wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.
21.a	21. The memory module of claim 16, further comprising:
21.b	a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit,
21.c	wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage,
21.d	wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the first pre-regulated voltage, and
21.e	wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage.
22	22. The memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output.
23.a	23. The memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and
23.b	wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
24.a	24. A memory module comprising:
24.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;
24.c	a voltage conversion circuit configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

Ref. #	Listing of Challenged Claims
24.d	[1] a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, [3] wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages; and
24.e	[1] a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage, [2] wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and [3] wherein the one or more operations include a write operation to transfer data into non-volatile memory.
25	25. The memory module of claim 24, wherein, in response to the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.
26.a	26. The memory module of claim 25, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and
26.b	wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.
27	27. The memory module of claim 26, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode.
28	28. The memory module of claim 27, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode.
29	29. The memory module of claim 24, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage or below a second predetermined threshold voltage.

Ref. #	Listing of Challenged Claims
30	30. The memory module of claim 29, wherein the first predetermined threshold voltage is above a specified operating voltage, and the second predetermined threshold voltage is below the specified operating voltage.

I. INTRODUCTION

The Institution Decision ("ID") correctly found all claims obvious. Netlist's Patent Owner Response ("POR") repeats many of the arguments that the ID already rejected.

II. ARGUMENT

A. There was no improper incorporation by reference (POR 1-2)

The Petition did not "improperly incorporat[e]" from the expert declaration, POR 1, as the ID correctly found, *see* ID 13, 35. The Petition provided cross references ***within the Petition*** for later limitations that were nearly identical to earlier limitations and thus "obvious for at least the same reasons ***above***."[1] Pet. 57-58, 68-70, 110-12, 123-25.

Similarly, Netlist is incorrect that the cross reference to claim 5 means there was no support for "an ***over***voltage condition as required by claim 7." POR 1-2 (citing Pet. 57). Claim 7 depends from claim 6, and the Petition's analysis of claim 6 explained that detecting both ***over-*** and under-voltage conditions was obvious. Pet. 52-55; *see also infra* pp.21-24. There was no need to repeat this analysis for dependent claim 7.

B. Construction of "memory module" (POR 2-4)

The Board properly found that Harris, the FBDIMM Standards, Amidi, and

[1] Unless otherwise noted, emphases are added and internal quotes are omitted.

Spiers all disclose a "memory module," ID 14, 15, 17-18, 29-33, 47-48, as explained by the Petition, Pet. 19-20, 77-78; *see also infra* pp.24-27. After institution, the District Court held that "*memory module*" in the preamble is "[l]imiting," EX2032, 35, consistent with the Board's assumption, ID 18 n.1. Contrary to Netlist's suggestion, the District Court did not further limit "*memory module*" to only "***main*** memory modules…designed to connect to the ***primary*** memory controller." POR 3-4. The District Court never used the words "main" or "primary." EX2032, 26-28. And the construction was simply that "*memory module*" (in the preamble) is "[l]imiting," without more. *Id.* 35.

Netlist misleadingly quotes statements by Dr. Wolfe about "***main*** memory modules," POR 3-4, but Dr. Wolfe explained that in the context of ***this*** patent, a "memory module" is ***not*** limited to main memory or to any specific connection, EX2060, 125:12-127:13 ("memory module" is "a circuit board that connects to a host computer that includes memory"); *see also* EX2056, 100:15-101:19 (similar).

C. Grounds 1-3 (POR 4-47)

The Board properly rejected Netlist's arguments about Grounds 1-3. ID 13-44.

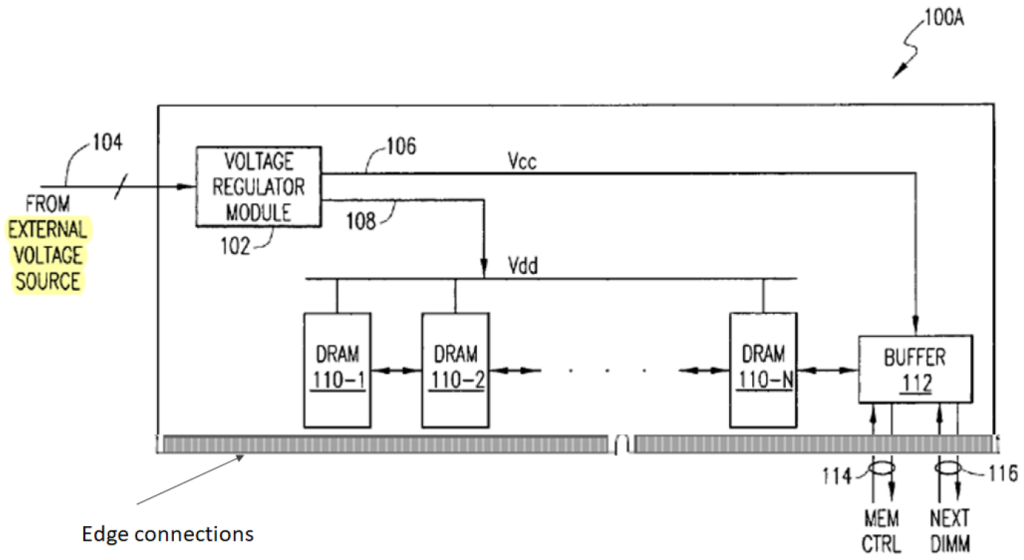
1. Ground 1 (Harris+FBDIMM Standards) discloses edge connections to receive power from the host system (POR 4-14)

The Board correctly found that Ground 1 (Harris+FBDIMM Standards)

teaches "*edge connections configured to couple* ***power****…signals*," rejecting arguments similar to those repeated by Netlist here. ID 18-20; POR 4-14.

Netlist does not dispute that the FBDIMM Standards (part of Ground 1) teach supplying power via edge connections, Pet. 16-21, and Netlist's expert admits that such edge connections were "standard," EX1075, 97:16-98:18, 163:16-20; EX1077, 9.

Netlist argues that Harris's reference to "***externally*** supplied voltage" (e.g., yellow below) requires power "external" to the ***entire*** "host system," POR 4-8, when it merely requires power "external" to the ***DIMM memory module*** (but still from the host system, including from edge connections as was well known), EX2060, 66:7-:19, 67:20-68:21, 91:22-92:7, 129:24-130:17; Pet. 21-22.



POR 7.

Netlist wrongly annotates Figure 1A (above) to suggest that Harris would

never utilize edge connections at the bottom for power, POR 6-7, but Figure 3 of Harris, below, illustrates memory boards 306 coupled to the host system ***only*** through their edge connections (red), meaning power would also come from those edge connections:

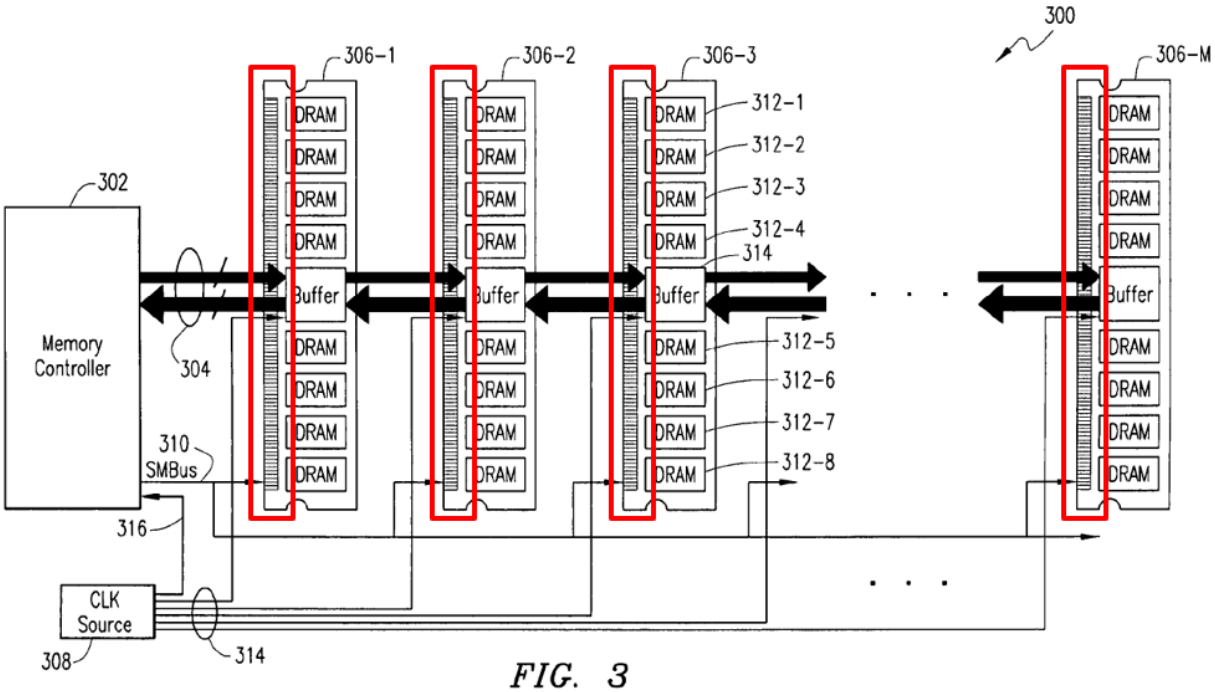


FIG. 3

EX1023, Fig.3. Indeed, Figure 3 of Harris above is nearly identical to a drawing by Intel where the memory modules admittedly receive power through the edge connections from the host system. EX1075, 171:4-:17; EX2101, 4. Harris also confirms that, "[a]lthough not explicitly shown in this FIGURE [3, above], each memory board also receives a supply voltage …[which] may be sourced from the memory controller 302 [which is part of the host system, EX1075, 167:23-168:1]

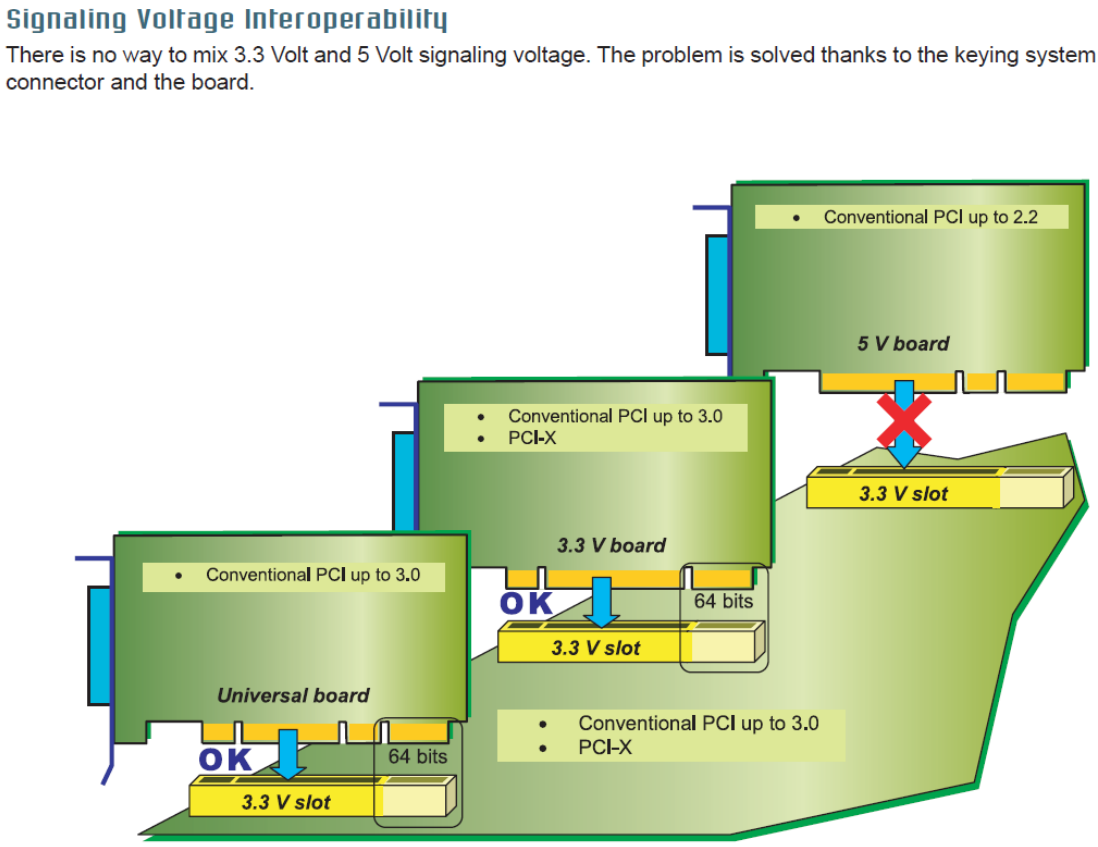
or from a separate voltage source." EX1023, [0017]. Netlist's argument that this disclosure of Harris is somehow erroneous, POR 11, is without merit since there is no dispute that the supply voltage was commonly provided through edge connectors "***alongside*** the memory controller signals," EX2060, 131:3-:5.

Netlist misinterprets paragraph [0019] of Harris to conclude that "Harris intentionally eliminates system board power" ***entirely***." POR 8. To the contrary, Harris proposes avoiding the need for ***different*** system board voltages — such as "3.3V, 2.5V, 1.8V, 1.5V and beyond," EX1023, [0002] — by simply supplying a ***single*** voltage (i.e., "12V")[2] to the memory module, *id.* [0012-13], so that an "on-board voltage regulator module [e.g., 102 above] [can] generate appropriate local

[2] Netlist's expert admitted that it was common at the time for the host system to provide a ***regulated*** "12V power supply." EX2061, ¶65; EX1075, 180:14-183:3; EX2038, 8, 13. Netlist argues that Harris is limited to receiving an ***unregulated*** 12V supply, POR 9-10, when in fact Harris teaches that the input voltage can be "***regulated*** or unregulated," EX1023 [0014]. Indeed, both experts agree that Harris's disclosure of a 12V supply with "wide tolerance (e.g., around +/-15%)," *id*. [0013], means that the voltage is ***regulated*** to stay within those limits. EX1003, ¶484; EX1075, 179:21-180:6, 183:7-184:11; EX2060, 65:23-66:6, 273:7-:12, 274:17-275:3.

voltage levels" on the memory module, *id.* [0003]. As Dr. Wolfe explained, Harris's "technology-independent voltage distribution scheme" eliminates the need for a "system-***board-specific*** power supply," *id.* [0019], therefore a module with "a new DRAM technology…could be plugged into the same DIMM slots because of this decoupling between the actual memory voltages [specific to a particular generation of memory chips on the module] and the voltage supplied by the slot," EX2060, 116:10-117:6.

Using edge connectors like those illustrated in Figure 3 above to supply power is also consistent with Harris's use of the known FB-DIMM ("FBD") design, except with "***few[er]***" power pins given the higher 12V input voltage. EX1023, [0012]; EX2060, 100:12-101:19, 102:17-:25, 103:11-104:23. To prevent "accidental damage" due to this change in the power pins of the edge connector, Harris teaches changing "the board's connector keyway" so that it is "not interchangeable with the standard DIMM." EX1023, [0013]; EX2060, 117:7-:21. This was a standard technique for memory modules receiving power ***from the host*** via the edge connections:



EX2016, 6-7; *see also* EX2101, 21-22; EX1075, 171:21-175:20. Harris's reference to using a "keyway" along the edge connections confirms that power would be coming from those edge connections, as was standard.

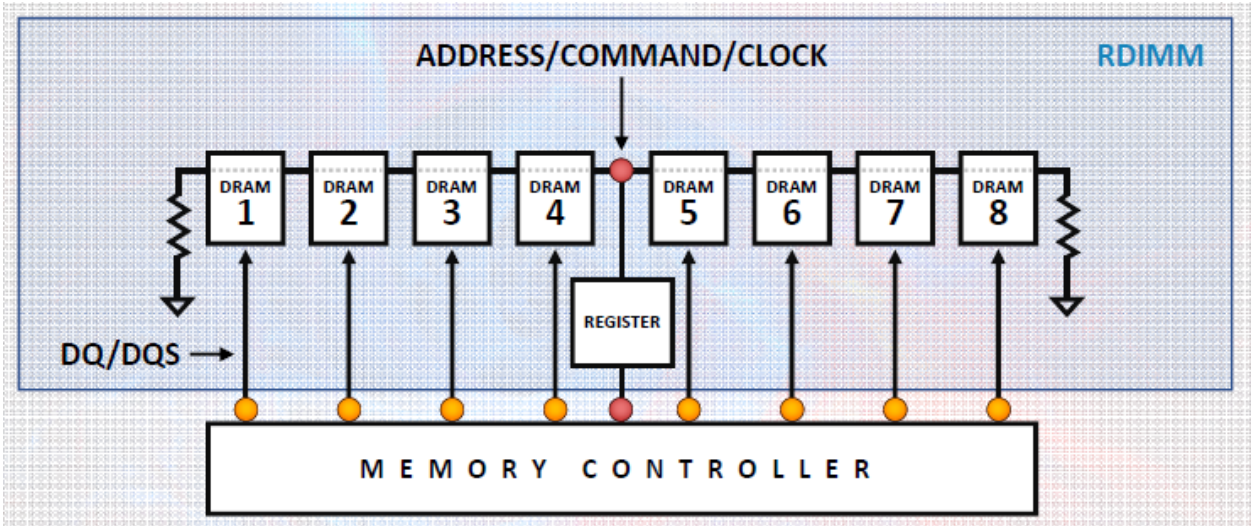
Netlist's argument that "[s]upplying power…from [the] ***side***…was known," POR 7, misses the point: regardless of whether a side connection was ***possible***, that would not negate the obviousness of using ***edge*** connections for power, as was highly common. *See Dome Pat. L.P. v. Lee*, 799 F.3d 1372, 1381 (Fed. Cir. 2015) (existence of a better alternative "does not mean that an inferior combination is inapt for obviousness purposes" (quoting *In re Mouttet*, 686 F.3d 1322, 1334 (Fed. Cir. 2012)). Indeed, Netlist's expert admitted that using ***both*** was a known option,

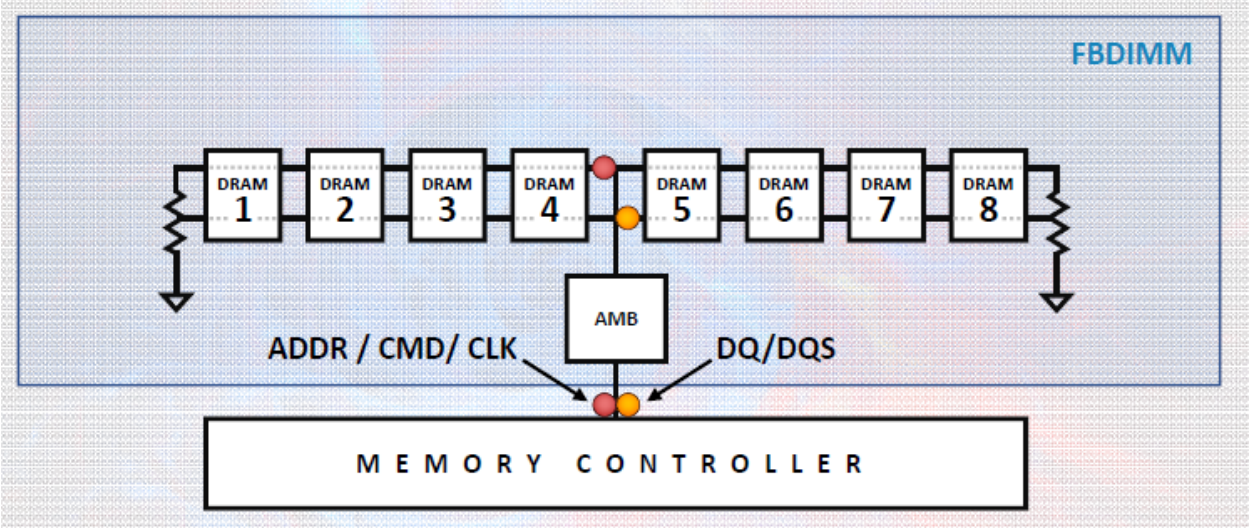
consistent with the combination for Grounds 2-3: the side connection could be used for battery backup (as taught by Amidi), and the edge connections could be used for power from the host system during normal operation (as taught by Harris):

EX2035, 39; EX1075, 165:10-166:12.

2. Harris discloses receiving "*data, address, and control signals*" from the host (POR 14-18)

As shown below by Netlist's technology tutorial, an FBDIMM (second below) receives ***signals*** for data (DQ), address (ADDR), and control (CMD), similar to an RDIMM memory module (first below):





EX1077, 8-9; EX1075, 91:23-92:19, 95:14-96:13, 97:16-98:18.

Netlist incorrectly argues that Harris's FBDIMM (or FBD) does ***not*** receive data, address, and control "signals" from the host system because, under the FBDIMM standard, those signals are ***encoded*** first into a packetized signal that can be sent to the AMB (shown above) on fewer wires than if the signals were all sent separately. POR 14; EX2061, ¶31; EX1075, 155:22-157:1; EX2060, 8:3-11:6. In essence, Netlist is trying to rewrite the claims (and its expert's testimony) to

require "***dedicated*** pins" for address, command, and data, EX1075, 212:3-:8, 213:3-215:20, 219:13-220:9, 226:7-228:8, even though that is not what the claims say, and the specification specifically identifies FBDIMM as an embodiment of the invention. EX1001, 21:46-:55 ("fully-buffered (FBDIMM)"). Excluding a preferred embodiment from the claims is "rarely, if ever correct." *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022).

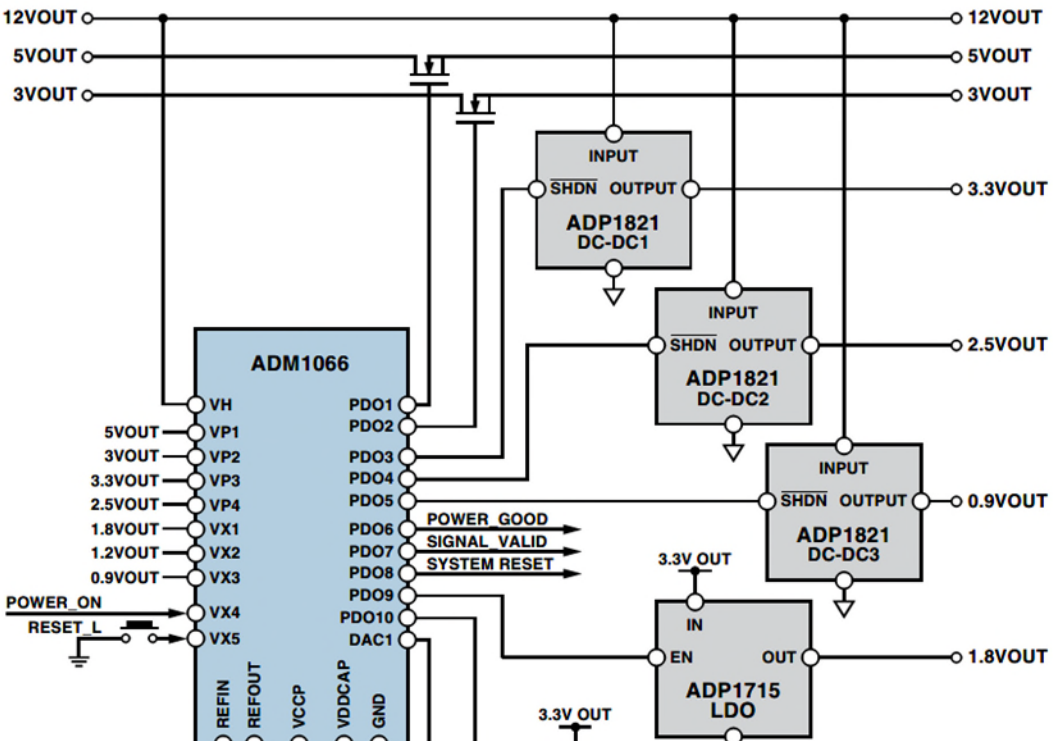
Indeed, Netlist concedes that the signals received by the AMB on the FBDIMM ***result*** in "data, address, and control ***signals*** needed by the DDR2 SDRAMs." EX2061, ¶31. And the FBDIMM standard confirms that "[a]ll memory control for the DRAM ***resides in the host***, including ***memory request initiation***," and the AMB "[a]cts as DRAM memory buffer for all ***read, write***, and configuration accesses addressed to the DIMM." EX1027, p.1. As a buffer for all such commands to the FBDIMM, the AMB must necessarily couple data, address, and control ***signals*** from the host system to the memory module—exactly like the claims require.

3. Harris and the FBDIMM Standards render obvious using *three* buck converters (POR 18-33)

The Board correctly rejected Netlist's argument, repeated here, that it was not obvious to use ***three*** buck converters. ID 21-23.

a) Harris is not limited to one or two buck converters (POR 20-24)

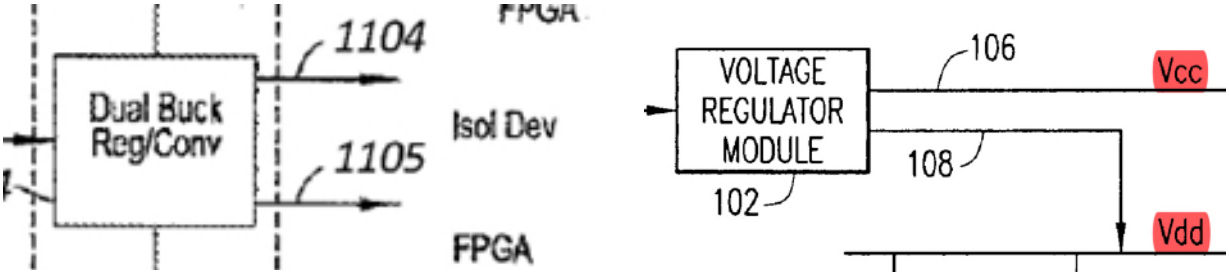
Netlist incorrectly argues that Harris only discloses "using a ***single*** converter." POR 20. But buck converters were well-known switching devices commonly used to step down an input voltage to a lower output voltage. Pet. 28-29. Netlist's expert agrees. EX1075, 103:21-107:14, 112:12-113:19. It therefore would have been obvious to a POSITA—and consistent with Harris—to use ***three*** buck converters to convert the 12V input to the three required voltages on the memory board. Pet. 27-30; EX2060, 53:16-54:14 ("Normally, if you need to generate multiple output voltages, you would use multiple regulators…"). This was common, as shown below. EX1062, 15 (below, showing three buck converters labeled ADP1821 coupled to one 12V input to generate 3.3V, 2.5V, and 0.9V outputs); EX1075, 132:21-141:23; EX1078, 1 (ADP1821 datasheet).



Netlist's argument that Harris only teaches a ***single*** buck converter is based on misreading the following sentence: "Preferably, ***a*** high-frequency switching voltage…may be implemented as the on-board VRM 102." POR 20 (citing EX1023, Fig.1A, [0010]). But in a patent like Harris, "a" means "one or more," *see, e.g.*, *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342-43 (Fed. Cir. 2008), as confirmed by paragraph [0010] and claims 1 and 30 of Harris ("at least one" VRM).

Furthermore, Figure 1A of Harris (below right) is very similar to the "dual-buck converter" in Figure 16 the 054 Patent (below left), which claim 15 of the 054 patent makes clear counts as "***two***…buck converters" (given the two different

outputs, just like Harris), not one buck converter as Netlist now argues:

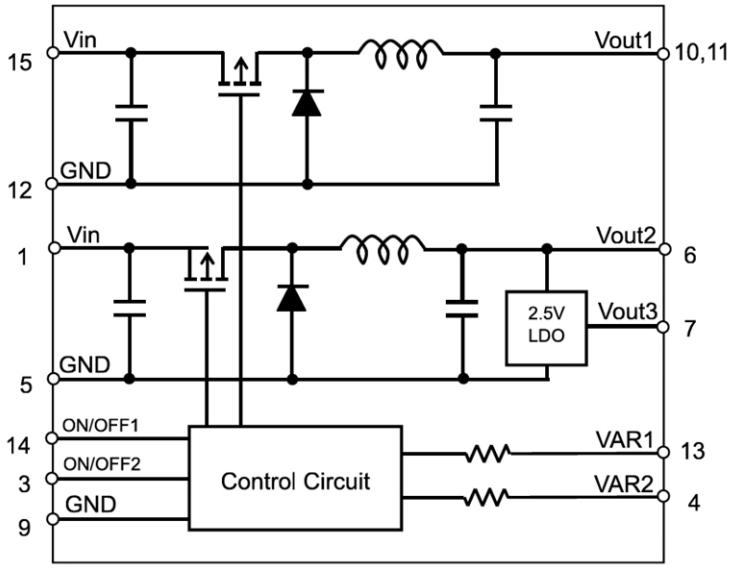


See also EX1075, 117:25-118:16. Indeed, the District Court, at Netlist's urging, construed "dual buck converter" to merely require "two regulated voltage outputs." EX2032, 18-21, 34; EX1075, 124:22-125:8, 126:9-:18; EX2060, 97:13-98:3. This further confirms that Figure 1A of Harris explicitly teaches at least ***two*** buck converters (for V_{CC} and V_{DD}, above right).

Netlist's attempt to define the number of converters based on the number of "inductors" (POR 20-21) lacks any support. *See generally* EX1001 (not mentioning "inductor"); EX2032 (same). In any event, it was well known that a single chip can include multiple buck converters (and inductors). *See, e.g.*, EX1048, 1-2 ("DC-DC converter"—singular—providing ***two*** regulated voltages, Vout1 and Vout2, from ***two*** buck converters, shown below); EX1075, 106:24-109:8 (discussing use of inductor in a buck converter); EX2060, 98:8-:18 (same); EX1058, 5, 14-15 (similar).

DC-DC Converter Specification(DRAFT)

MPD4S014S



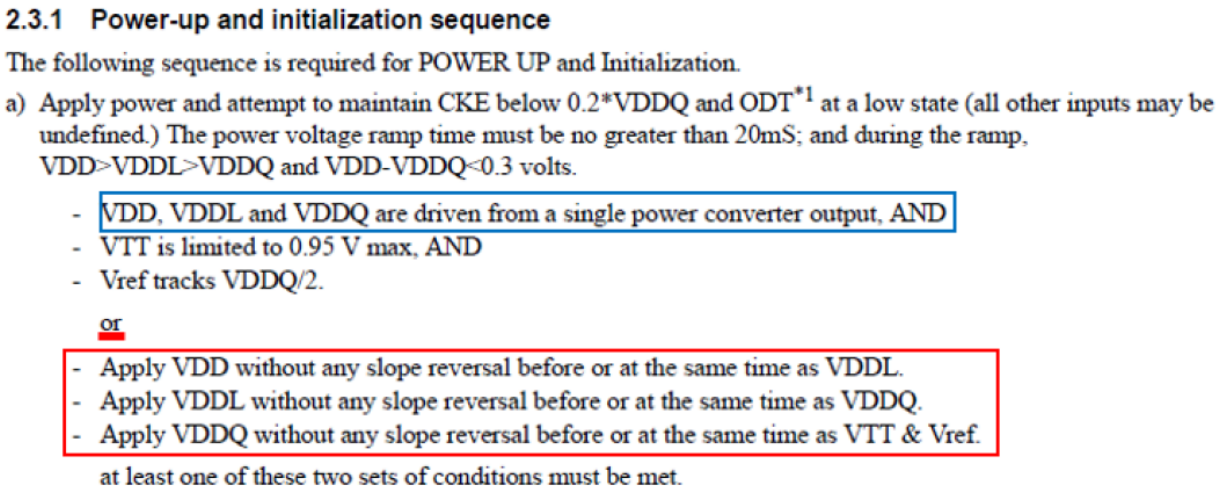
See also EX1075, 127:21-129:24, 228:25-232:19; EX1042, 16 (corresponding to EX1048, 2).

Finally, the alleged space required for multiple buck converters, POR 21-24, is not even mentioned in the 054 Patent or its claims, since solving any such problem was within the level of ordinary skill, EX2060, 53:16-54:14, 89:1-:21; *infra* pp.20-21.

b) It was obvious to use different converters for voltages that have different functions (POR 24-30)

The Board correctly found it obvious to use different buck converters for different voltages (e.g., V_{DD} vs. V_{DDL}). ID 22-23. JEDEC clearly teaches this as an option (e.g., red below) instead of using "a ***single*** power converter" for those

voltages (blue below):



2.3.1 Power-up and initialization sequence

The following sequence is required for POWER UP and Initialization.

a) Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT*1 at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2.

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

POR 28 (quoting EX1026, 9 (DDR2)); *see also* EX1046, 15 (same for DDR3).

Netlist argues that using a ***single*** converter (as shown in blue above) was more common, POR 24-30, but the Petition explained the motivation for ***multiple*** converters (e.g., red above), including because the JEDEC standards treat those voltages separately, thus permitting power-on sequencing; providing independent control; improving efficiency; and saving power. Pet. 29-30. Netlist's example with a "***single*** power source" is ***not*** for an FBDIMM like Harris. POR 26 (citing EX2006, 3-4 ("SODIMM")); EX1075, 102:17-103:9 (SODIMM is unbuffered as shown in EX2045 and EX2046, 4.20.11-23).

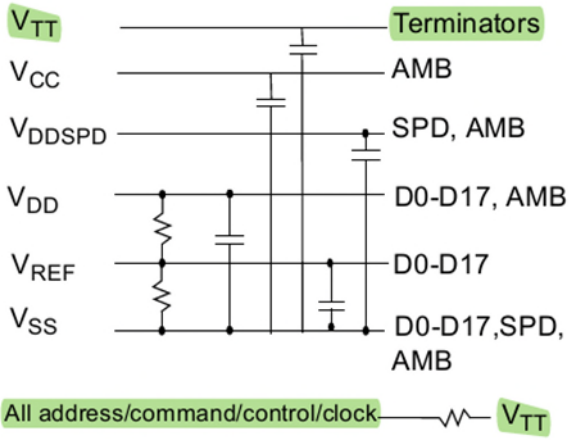
Netlist argues the JEDEC standard above is for the memory ***device*** (not module), POR 26-27, but Harris teaches a module that supplies all the voltages needed on the module, which would include all those above needed by the memory devices. EX2060, 37:13-38:5 ("because there is a separate voltage regulator

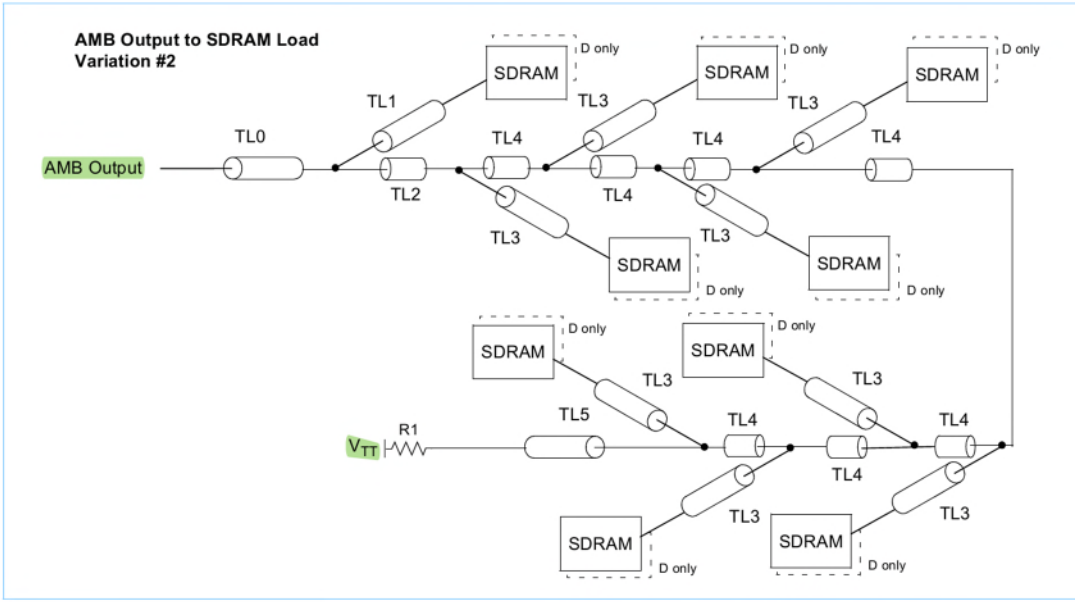
module, one would build their own connections … [including] three discrete connections"). Similarly, Netlist argues that JEDEC's express recommendation of ***sequencing*** the different voltages (red above) does not ***require*** separate converters, POR 27-30, but that was the obvious way, and came with several benefits (including for V_{CC} vs. V_{CCFBD}). EX1003, ¶255; EX2060, 39:2-:10 (allows "sequenc[ing] the power," "turn[ing] the power on and off independently," and saving "cost"), 44:25-46:10 ("eliminate[s] cross-coupling of noise" and can solve "spacing constraints"); EX1075, 134:22-136:2, 194:23-195:7; EX1062, 13-15 ("sequence"/"sequencing"); EX2012, 73 ("sequencing").

c) It was obvious to use a third buck converter for V_{TT} (POR 30-33)

With respect to V_{TT}, Netlist argues that it would not be generated on Harris's module because V_{TT} is not explicitly listed by Harris, and V_{TT} could be supplied from the motherboard instead. POR 30-32. But Harris teaches generating ***all*** the voltages on the module, including all of the voltages for an FBDIMM ("FBD"), which would include V_{TT}, as the Board found. ID 20-23; EX1023, [0012]; EX2060, 30:15-:20, 72:22-73:7, 103:11-104:23 ("the 36 power pins [replaced by Harris's 'local conversion to V_{dd}']…include the VTT pins"), 109:5-111:10, 239:8-:20. In particular, Harris's module provides the voltages for the buffer 112 to send address and control signals to the DDR memory devices, which the FBDIMM Standards make clear require not just V_{DD}, but also V_{TT} to terminate those signals.

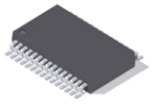
Pet. 17-18; EX1028, 9, 15, 68 (below).





Furthermore, V_{TT} is required by JEDEC to track V_{DD} (which is clearly produced on Harris's module, as shown in Figure 1A), which is why dual buck converters for generating V_{DD} and V_{TT} were readily available. EX1028, 9 ("(DRAM Interface VTT)…should track as 0.5 * 1.8 volt supply"); EX2060, 72:22-73:7, 196:3-197:7 (citing EX1040-41, EX1048).

TEXAS INSTRUMENTS



TPS51020

SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS

- Notebook Computers System Bus and I/O
- DDR I or DDR II Termination

EX1040, 1.

DUAL MODE AND DDR MODE

TPS51020 provides one-chip solution for system power supply, such as for 5 V, 3.3 V or 1.8 V, and a dual switcher DDR power supply. By simply selecting $\overline{DDR}$ signal and some external configuration change following the instructions below, TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT} source/sink capability and V_{TT} reference output.

Id. 11.

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

- Complete DDR Memory power solution
  - VTT Tracks VDDQ/2
  - VDDQ/2 Buffered Reference Output
- Supports DDR-II and HSTL

Applications

- DDR V_{DDQ} and V_{TT} voltage generation
- Desktop computer
- Graphics cards

EX1041, 1.

Netlist's suggestion of producing V_{TT} on the motherboard — where V_{TT} could change with each new generation of memory devices — would defeat the benefit of Harris's invention, e.g., "a technology-independent voltage distribution scheme" to "provide upgrades to next generation DRAM technology in a cost-effective manner." EX1023, [0019], [0002].

Netlist also argues that an LDO linear regulator could generate V_{TT} instead of a buck converter, POR 33, but as shown above, buck converters were commercially available for V_{TT} and provided high efficiency compared to an LDO. EX1075, 112:12-114:8 (LDO may be only 10% efficient); EX2060, 57:17-:20, 58:18-59:10 (buck converters up to 98% efficient), 140:15-:24 (trend has been to use buck converters).

4. It was obvious to combine Amidi's battery backup with Harris (POR 34-40)

For Grounds 2-3, the Board correctly found a motivation to combine Amidi's battery backup with Harris. ID 29-33; Pet. 41-45. Netlist argues Amidi was not needed because Harris already had a solution of redundant power supplies to deal with power failures. POR 34-36. But Amidi provided a redundant power

supply on the module itself — completely independent from the host — which differs from Harris's redundant power sources that were provided by the host (and thus subject to the host losing power). Pet. 41-42; EX1003, ¶172; EX1024, 1:28-35, 2:6-26.

Netlist also argues that such a battery back-up on the module is complex, can keep the data for a limited time only, and requires substantial on-board space. POR 37-40. But such on-board battery backup systems were well-known at the time since their advantages "can be very helpful," EX1024, 2:6-26, as evidenced by Amidi and Netlist's own BBvault memory module from years earlier:

May 2005 . . . . . 1st BBvault shipped (battery-backed cache module). In production w/ 3rd generation.

BBvault

EX2035, 39; EX1075, 165:10-167:7. Furthermore, even if the battery backup takes one side of Harris's FBDIMM, the other side can still include one rank, or even two ranks using ***stacked*** memory devices (which save space). EX1028, 36 ("Components shall be surface mounted on ***one*** or both sides of the PCB.");

EX1075, 74:22-75:25 ("you've now doubled the amount of memory stored in the same amount of physical space"), 77:10-:17.

5. Overvoltage protection for claims 6, 9, 17 (POR 40-45)

The Board correctly found ***over***voltage protection in claims 6, 9, and 17 obvious in light of Grounds 2-3. ID 35, 42-44. Netlist incorrectly argues that the Petition failed to show predictable results for handling over-voltage conditions, POR 40-41, ignoring the Petition's extensive explanation and evidence about a POSITA's understanding of how to handle power anomalies, including both under- and over-voltage conditions, with a reasonable expectation of success. *See, e.g.*, Pet. 12-13, 41-45, 53-54, 70-72; EX1003, ¶¶138, 345-55. The Petition also explained how Amidi, in combination with Harris (Ground 2) and Hajeck (Ground 3), teaches a trigger signal to switch to back-up power and avoid data loss in case of a "power fault," including under- and over-voltage conditions. *Id.*; *see also* Pet. 49-50; EX1003, ¶¶315-321; EX2060, 226:16-:22, 230:17-232:6, 251:10-254:2 (explaining Hajeck). Netlist's arguments to the contrary attack the references individually (e.g., for lacking a trigger signal), while ignoring the proposed combinations. POR 41-45.

Netlist argues the prior art only solved ***under***voltage problems, and thus did not provide a motivation to switch to back-up in case of ***over***voltage. POR 41-45. To the contrary, neither Harris nor Amidi is limited to handling ***under***voltage

conditions. Harris expressly teaches that its memory module can "***accommodate[]***" up to a 15% variation above and below the nominal 12V supply voltage, EX1023, [0013], which would have motivated a POSITA to detect when the voltage is outside of the +/-15% tolerance not accommodated by Harris's module, EX1003, ¶¶347-52. And Amidi teaches "power fault detection" for memory modules in general, with undervoltage detection being only an example. EX1024, Title, Abstract, 2:6-:19 ("power fault detection for a memory module may be provided in a variety of ways"). Dr. Wolfe explained that a POSITA understood the dangers of both under- and overvoltage. EX1003, ¶¶350-52; EX2060, 254:24-256:11, 258:12-:20; EX1065, [0018-19] (alarm signal when voltage is outside of a range, including upper and lower thresholds); EX1063, 1-2 (PCI Power Supervisor detecting Over-, Under-, and out-of-window voltage faults); EX1061, 15 (similar); EX1062, 15 (similar). Netlist's expert agreed that power spikes were known power anomalies at the time. EX1075, 196:10-197:13.

Netlist, ignoring the nature of power supply anomalies, such as power surges, argues that overvoltage poses no danger. POR 42-44. But the Petition explained, e.g., with reference to Hajeck, the problems caused by over-voltage anomalies, such as power surges, that can cause data loss, data corruption or circuitry damage in memory boards — as anyone with a surge protector at home knows. Pet. 70-71; EX1003, ¶¶138, 185. As discussed above, Harris also

discloses that its module can accommodate only +/-15%, which is consistent with some commercial converters requiring a V_{CC} input voltage with a 5% tolerance for proper operation and an absolute maximum of 30% overvoltage "beyond which the device may be damaged." EX1041, 4 (below in part).

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired Functional operation under these conditions is not implied.

Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage			6.5	V
VIN			18	V

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VIN				16	V

6. Controller for claims 5, 7–8, 23–24 (POR 46-47)

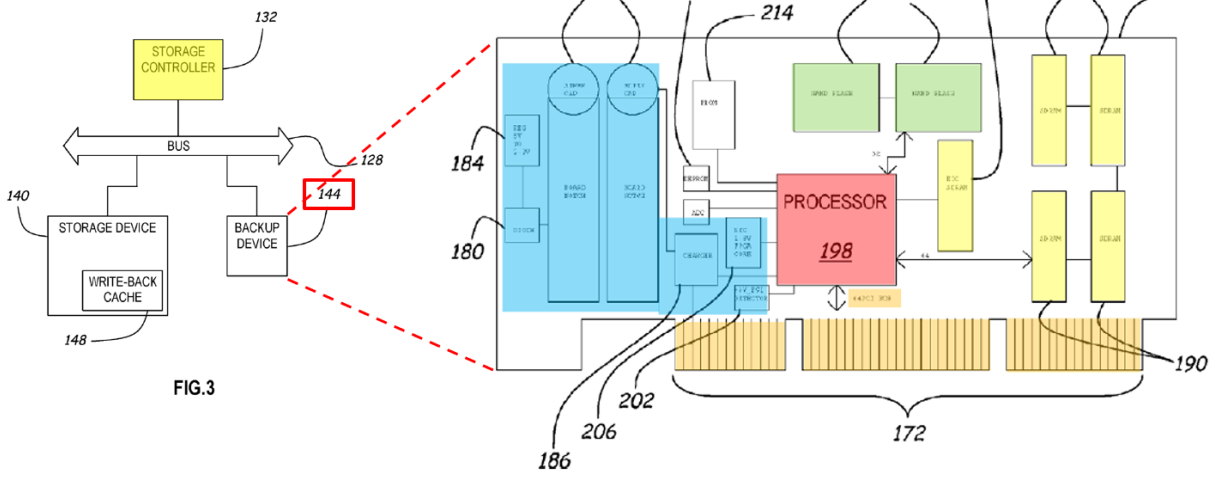
Netlist misleadingly argues that Grounds 1-3 lack the "*controller*" to cause the S3 sleep mode, because conventionally this mode is initiated by the system controller, which is outside of the memory module. POR 46-47. But this argument ignores the combination of FBDIMM's S3 mode in Harris with Amidi's teaching of backup power management and logic functionality on the memory module to "maintain memory (through refresh, for example)." Pet. 43-44, 50-52; ID 35, 36; EX1024, 2:16-:19, Fig.11; EX1003, ¶¶175-77. In case of a power failure, Amidi's logic disconnects the system memory controller from the module, EX1003, ¶¶329-30, so a POSITA "would have been motivated to use the S3 mode

of buffer 112 [on Harris's module] when implementing the backup power supply and logic functionality as disclosed in Amidi, because S3 mode performs the function of refreshing the memory (e.g., self refresh), just like in Amidi," *id.* ¶330.

D. Grounds 4-5 (POR 47-75)

1. Spiers's PCI card is a "*memory module*" (POR 47-51)

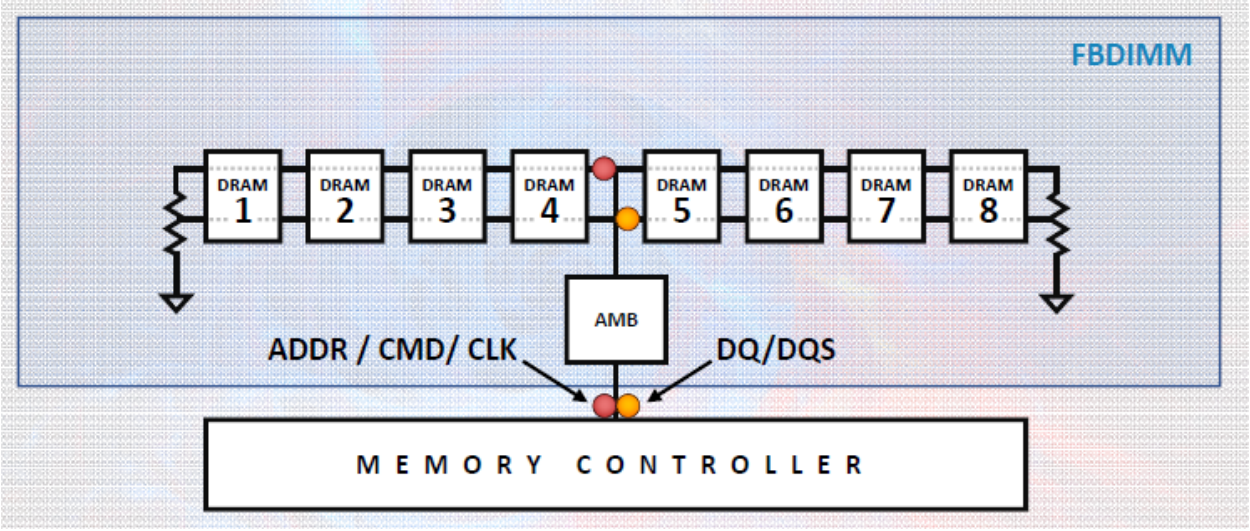
The backup device 144 in Spiers, which is implemented in the PCI card shown in Figure 5, satisfies the District Court's construction for "*memory module*" discussed above (pp.1-2) because it connects over a "bus" to a "memory controller" in the "storage controller" 132, which sends memory commands to the backup device 144, as shown below. EX2060, 213:1-:8, 213:14-:22, 206:6-207:13.



EX1025, Figs.3, 5, [0034] ("[T]he storage controller 132 [in Fig.3 above left] stores a copy of the data in the backup device 144….[T]he storage controller periodically flushes the data stored in the backup device 144…."); EX1003, ¶¶598-

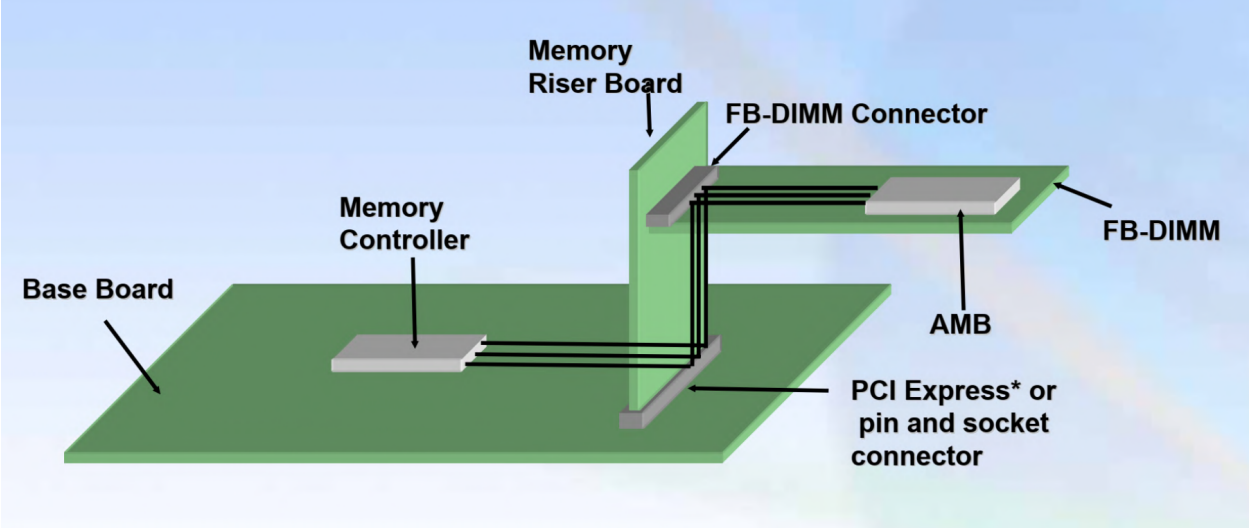
99; Pet. 77-78.

Indeed, it was well known that PCI cards could be "memory modules," as recognized by the PCI standard itself. EX1031, 1 ("The [PCI] bus is intended for…processor/***memory*** systems."), 22-25 (describing Memory Read and Write commands); EX2060, 177:25-179:9. Netlist concedes that parts of Spiers's PCI backup device 144 (e.g., SDRAM 190 or flash modules 194) "include the necessary structure to connect to a memory controller." POR 48. Netlist's position appears to be that the intervening processor 198 on Spiers's PCI card prevents the PCI card from functioning as a "memory module," but the use of an intervening processing unit on the "memory module" that is configured to interact with the "memory controller" of the host system is a common feature of well-known "memory modules," such as an FBDIMM (below), where the "AMB" has an interfacing function similar to processor 198 in Spiers's PCI card:



See EX1077, 9; EX1075, 97:16- 98:18; *see also id.* 91:23-92:19, 95:14-96:13 (similar for RDIMM). As discussed above (pp.9-10), FBDIMM is a disclosed embodiment of the 054 Patent, so excluding it from the scope of the claims would "rarely, if ever [be] correct." For similar reasons, it would be incorrect to exclude Spiers's PCI card from the scope of the claims simply because it has a "processor" on the module (similar to the AMB on an FBDIMM) that interacts with the "memory controller" in "storage controller" 132.

Lastly, Netlist is wrong to suggest that the ***slot*** used for a PCI card precludes the PCI card from being a "memory module." POR 49-51. Neither the District Court's construction for "*memory module*" (pp.1-2) nor the 054 Patent puts any limitations on the form factor or connector used by the memory module. *See, e.g.*, EX1001, 21:51-:55 ("… certain non-DIMM form factors are possible such as, for example…multi-media card (MMC), and small computer system interface (SCSI)"). Netlist's own exhibit includes an example configuration where a memory controller communicates with an FBDIMM through a PCI bus using a PCI connector:



EX2101, 14; EX1075, 198:11-200:7. This further confirms that a PCI card (such as Figure 5 of Spiers) can be used in conjunction with a memory controller in the host system.

2. Spiers+Amidi renders obvious three regulated voltages (POR 51-63)

The Board correctly found that Grounds 4-5 (with Spiers+Amidi) render obvious ***three*** regulated voltages. ID 49-50; Pet. 72-77.

a) Spiers is not limited to older SDR SDRAM memory (POR 51-56)

Netlist does not dispute that DDR2 and DDR3 were well-known types of SDRAM, and that Amidi teaches the use of DDR2 SDRAM memory devices. Pet. 31-32, 72-74, 90. But Netlist nonetheless asserts that a POSITA would not consider DDR2 and DDR3 to be suitable for use with Spiers. POR 51-56. The Board correctly rejected this argument. ID 46-47.

The only basis for Netlist's argument appears to be the specific voltages

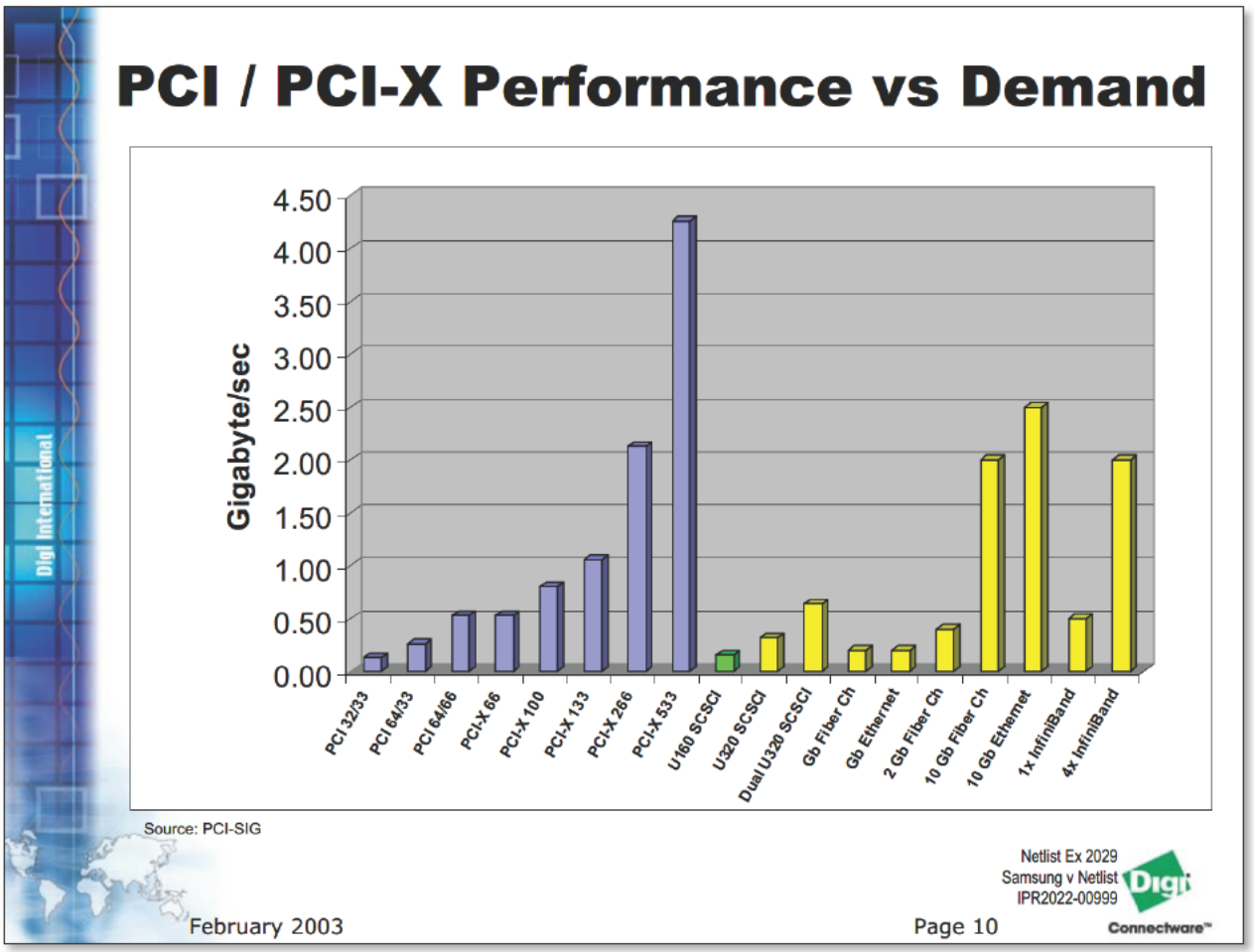
disclosed in Spiers. POR 51-56. Netlist repeatedly emphasizes that Spiers suggests using a 3.3V regulator, while DDR2 and DDR3 use lower voltages. *Id.* 52 (citing EX1025, Fig.5, [0037]). But lower voltages are a ***motivation*** for using DDR2 or DDR3—not a problem. As Netlist's expert testified, "lowering the voltage will [result] in lowering the power consumption, and that's just — that's an incredibly consistent fact, ***motivation*** in the industry." EX1075, 79:9-80:2.

b) It would be obvious to use newer, more efficient DDR2/DDR3 memory (POR 56-63)

Netlist's assertion that a POSITA would not be motivated (e.g., by Amidi) to use the faster and more advanced DDR2 or DDR3 devices in Spiers defies logic. It is well established that DDR2 and DDR3 provide substantial upgrades in speed and performance compared to older approaches like SDR. *See* EX2012, 70 ("less heat…more efficiency"), 73 ("usage is expected to increase to 80 percent [of all electronic systems]"); EX2060, 150:14-151:16, 180:8-182:11, 183:24-184:9, 245:4-246:8 (listing benefits for using newer DDR2 or DDR3 SDRAMs on Spiers's PCI card); *see also* EX1075, 86:12-89:11 (agreeing that "going from DDR1 to DDR2 to DDR3, the clock speed got faster with each new generation" and explaining that "all things being equal, if you increase the clock speed, you will increase the performance of the device"). And the Federal Circuit has recognized that there is "an implicit motivation to combine to make a device more desirable, for example because it is…faster…or more efficient." *Intel Corp. v.*

Qualcomm Inc., 21 F.4th 784, 797 (Fed. Cir. 2021) (rejecting Board's contrary finding).

Netlist's argument that the PCI connections in Spiers eliminate any need for the faster speeds provided by DDR2 or DDR3 is also incorrect. POR 58-59. Netlist's expert admitted that there were known, faster versions of PCI that "could be used in systems that use any of those technologies [including Ethernet] without necessarily being a bottleneck[.]" EX1075, 59:13-:23. The relative speed of these versions of PCI is illustrated in purple in an exhibit Netlist submitted, dated 2003:



EX2029, 10. Netlist's expert further confirmed that these advanced versions of PCI were intended to be backwards compatible, which means that any previous application using PCI could be adapted to use the faster version as well. *See* EX1075, 52:8-:25, 53:25-54:23. Given that the newer iterations of PCI could take advantage of the faster speeds provided by DDR2 and DDR3, a POSITA would have been motivated to implement those approaches in Spiers.

In addition to ignoring the level of skill at the time, Netlist's arguments are also incorrect legally because it is not necessary to show that using DDR2 or DDR3 would be the "***best***" implementation of Spiers, just that they were a "***suitable*** option." *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023) (reversing Board); ID 46-47.

3. It would be obvious to use three buck converters with Spiers+Amidi (POR 63-72)

The Board correctly found that Grounds 4-5 (with Spiers+Amidi) render obvious using ***three*** buck converters. ID 49-50; Pet. 72-77, 85-88.

a) Buck converter for V_{TT} (POR 63-66)

Netlist argues Spiers would not include V_{TT} because that voltage is (according to Netlist) only used for DDR3 devices in AC measurements and tests. POR 63-64. To the contrary, as discussed above (pp.16-19), a memory module (like Spiers's) with on-board power generation needs to use V_{TT} to terminate the address and control signals sent from the module's local controller to the

DDR2/DDR3 SDRAM devices. *See also* EX1003, ¶¶627-28, 630; EX1046, 15 (DDR3: "Apply VDDQ…before or at the same time as VTT & Vref"); EX1026, 9 (same for DDR2); EX1047, 2:7-:15 ("In…a dual-data-rate (DDR) memory system…a second supply voltage will be…one-half[] of a first supply voltage."), 5:56-:59 ("Vout2 may provide a VTT supply voltage").

Netlist's argument that Spiers is not an FBDIMM misses the point in the Petition. POR 65. The Petition referenced FBDIMM to explain that Spiers's processor 198 is interfacing with the SDRAM memories on the module "just like in an FBDIMM," creating the need for V_{TT}. Pet. 83; EX1003, ¶¶629-31. Finally, Netlist argues that an LDO could be used instead of a buck converter, POR 65-66, but as discussed above (pp.17-19), efficient dual buck converters were commercially available for V_{DD} and V_{TT}.

b) Multiple 1.8V buck converters (POR 66-67)

Netlist argues that a 1.8V voltage for V_{CCFPGA} and V_{DD}/V_{DDQ} could be provided from the same converter. POR 66-67. But as discussed above (pp.11-12, 14-16), a POSITA understood that using separate buck converters was a readily available and obvious design choice that provided a number of advantages, including efficiency, flexible sequencing, power control, and power savings. Even if an alternative implementation could be configured with a single converter, this does not make the use of separate converters non-obvious. *See, e.g.*, *PACT XPP*,

61 F.4th at 1380-81 ("suitable option"); *Dome Pat.*, 799 F.3d at 1381.

c) Two buck converters for 1.5V and 1.8V (POR 67-68)

Netlist's arguments regarding the use of two converters for 1.5V and 1.8V are wrong for at least the same reasons stated in the section directly above regarding the use of multiple buck converters outputting 1.8V.

d) Buck converter for 5V-to-3.3V (POR 68-72)

Netlist argues it was not obvious to implement Spiers's 5V-to-3.3V regulator as a buck converter because an LDO would be sufficient based on its expert's calculation. POR 68-72 (citing EX2061, ¶¶162-69).[3] That calculation, however, is based on incorrect assumptions, such as basing the calculation on a write-back

[3] Netlist also incorrectly asserts that the 5.5V-to-3.3V regulator 184 in Spiers is only "for use '***in the event of a power failure***." POR 68. But as Dr. Wolfe explained, regulator 184 is also used in normal mode. EX2060, 149:11-150:1 ("you're always using 184 because what's being monitored is the 5 volt supply, not the 3.3 volt supply, and the 5 volt supply feeds into 184"); *see also id.* 154:22-156:15, 156:23-157:8, 278:5-:15 ("it would…be obvious to have the regulator operate all the time"), 278:17-281:17 ("all the indications in Spiers [including diode 180] are that that 3.3 volts comes from the 5 volt to 3.3 regulator [184]"), 282:7-:14.

cache (like 148, orange below), *see* EX2061, ¶163, instead of Spiers's backup device 144 (green below).

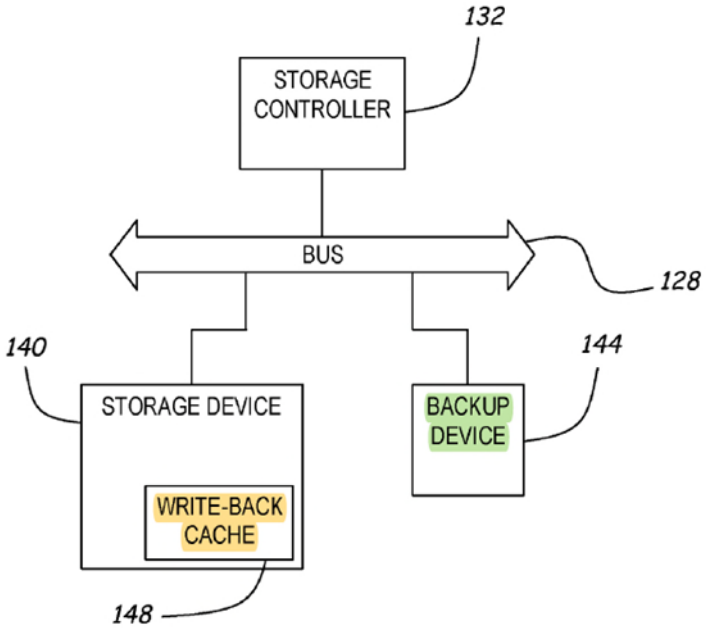
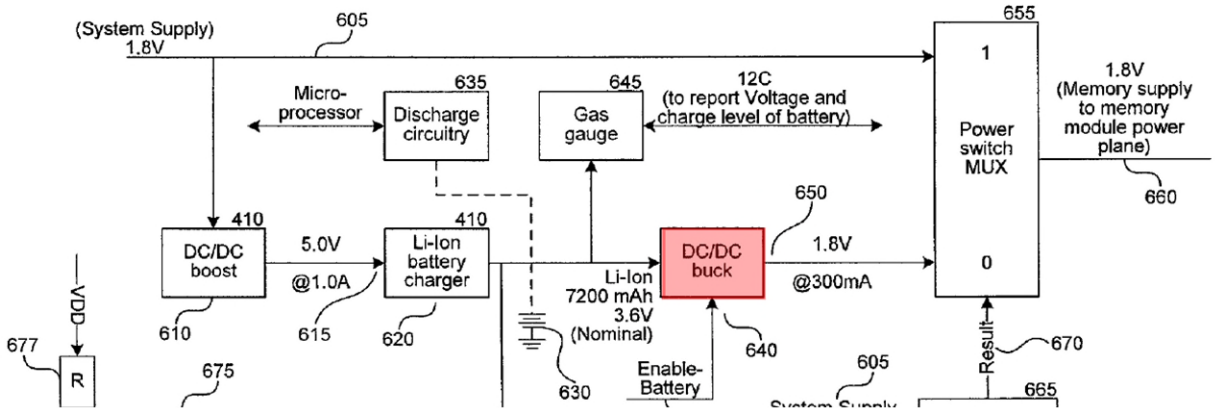


FIG.3

EX1025, Fig.3; EX1075, 208:20-209:1. Furthermore, using a buck converter for battery backup power is expressly taught by Amidi:



EX1024, Fig.6; Pet. 86. Netlist also argues that low-dropout buck converters had

"drawbacks," POR 70-72, but reliable buck converters for 5V-to-3.3V were commercially available at the time, *e.g.*, EX1048, 3 (requiring minimum input of 4.5V, minimum voltage drop of 1V, and minimum load current of 0A).

4. Claims 6 and 17 (POR 72-74)

Netlist repeats for Spiers the same arguments about the alleged lack of ***over***voltage protection, and elements missing from individual references (ignoring the combination), as discussed above (pp.21-23). POR 72-74. Contrary to Netlist's arguments, POR 73, Spiers is not limited to switching to backup power in case of ***under***voltage, but concerns "power failure, or other failure" in general, *see* EX1025, Fig.14 (step 720, "Power Fail Detect"), [0030] ("store the data in a non-volatile memory, such that if a power failure, ***or other failure***, occurs"). In fact, Spiers discloses a PCI 5V voltage detector 202, *see id.* Figs.5, 14, [0037], and such commercially available detectors included ***both*** under and overvoltage detection, *see* Pet. 107-08; EX1063, pp.1-2 (below); EX1003, ¶¶709-23.

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

Netlist argues that detecting overvoltage does not render obvious switching to backup power, POR 73, but that ignores the dangers of losing data (or damaging the circuit) due to the overvoltage, as discussed above (pp.21-23). Netlist also argues that, instead of Spiers's power circuit, Hajeck's ***charge pump*** could be used, POR 73-74, but that charge pump could handle only "a ***brief*** interruption, drop, increase, or spike in the voltage V_{IN}," EX1038, 3:2-:6; EX2060, 226:16-:22, 230:17-232:6, 251:10-254:2. In any event, the existence of an alternative does not make switching to backup power non-obvious, certainly not in "mission critical" systems relying on "irreplaceable data" as taught by Amidi. EX1024, 1:19-:20. And, of course, Hajeck's charge pump cannot operate "indefinitely" for all possible power anomalies. EX1075, 197:14-198:5.

5. Claim 9 (POR 74-75)

Netlist repeats its argument that the prior art lacks ***over***voltage detection and a corresponding signal transmission on the module itself. POR 74-75. But Spiers's voltage detector 202 would send an overvoltage detection signal to the processor, EX1003, ¶¶752-58, 785, 791, since a POSITA understood the dangers of overvoltage as discussed above (pp.21-23); *see also* EX1038, 1:10-:13 ("The…invention relates to…protecting storage subsystems…from ***damage and data loss*** caused by ***irregularities*** in a power signal provided by a host").

E. Claims 18-22 and 26-28 (POR 75-76)

For claims 18 and 26, Netlist appears to entirely misapprehend the mappings in the Petition. POR 75-76. The Petition correctly identifies a first (e.g., during normal operation, with power from the system) and second (e.g., during battery/capacitor backup power) pre-regulated[4] voltage for the first and second

[4] In the related 918 Patent, the District Court construed "pre-regulated input voltage" to have its plain and ordinary meaning, EX2032, 21-22, 34, similar to the Board, ID 38-39, and rejected Samsung's argument that the voltage must be pre-regulated ***on*** the memory module, EX2060, 268:18-270:5. Netlist's expert does not dispute the District Court's construction. EX1075, 142:10-144:18. Both

operable states in each Ground. *See* Pet. 63-65, 118-20. For dependent claims 19-22 and 27-28, the Petition correctly addressed these limitations, including the first and second diodes (yellow and orange, below, respectively). *See* Pet. 65-70, 121-25.

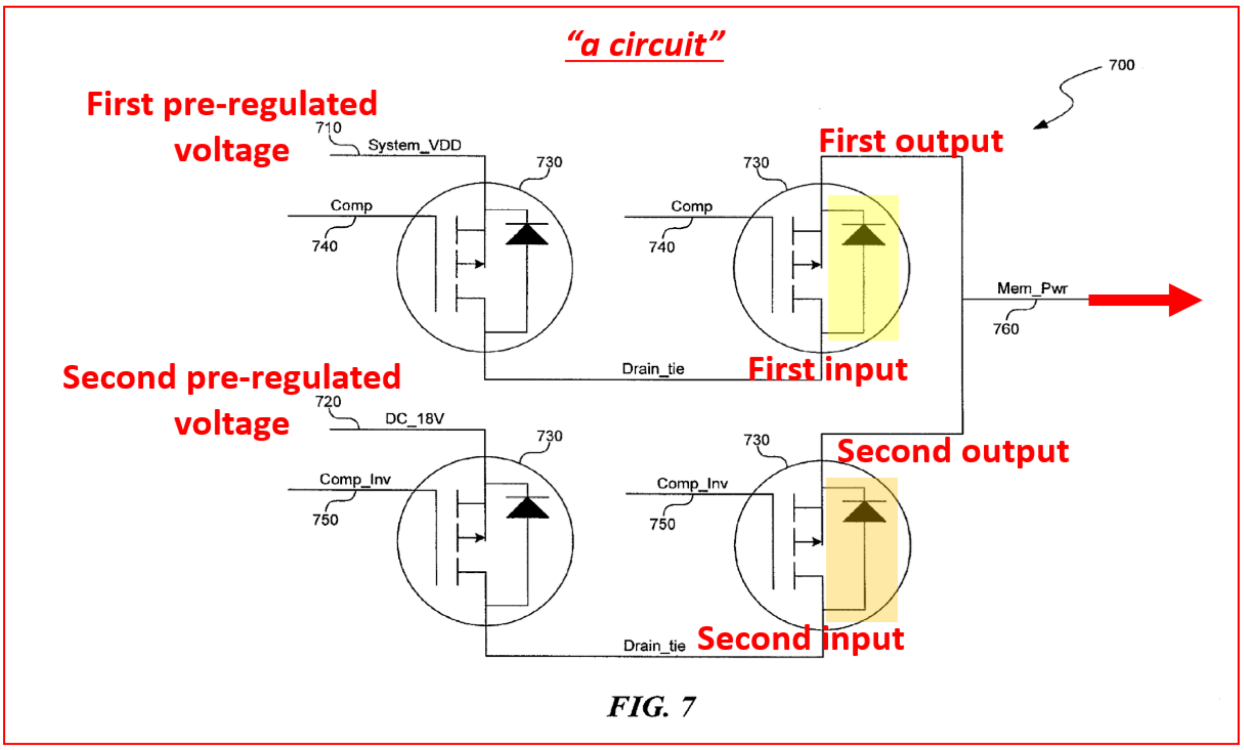


FIG. 7

III. CONCLUSION

For the reasons set forth above and in the Petition, Samsung respectfully requests that claims 1-30 be canceled as unpatentable.

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experts agree that the 12V input to Harris can be pre-regulated under that construction. *See supra* p.5, note 2.

Dated: June 20, 2023

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CERTIFICATE OF COMPLIANCE

I hereby certify that this **Petitioner's Reply to Patent Owner's Response** complies with the type-volume limitations of 37 C.F.R. § 42.24(c)(1) because it contains 5,598 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the reply exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 20th day of June, 2023, **Petitioner's Reply to Patent Owner's Response** and **Exhibits 1075 to 1078** were served by email on the following counsel for Patent Owner:

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